REMARKS

Telephonic Interview

Applicant's attorney appreciates the Examiner's telephonic interview of December 4, 2006, wherein the Examiner believed that further review of a Proposed Amendment as herein submitted might indicate that the 35 U.S.C. §102(e) rejections could be overcome.

Allowable Subject Matter

The following is an Examiner's Statement of Reasons for Allowance: Claims 13 and 19 are allowable over the prior art of record.

> "As to claims 13 and 19 the limitations are comprehensive in that all limitation of the other claims were presented. These limitations if taken separately or in combination are anticipated by prior art, however taken together they produce an environment for improving client/server system performance and quality of services of a network server by incorporating a network interface for processes [sic] incoming messages sent by a client device to a network server in a novel way. The examiner has found that the prior art of record does not teach or suggest or render obvious novel claims 13 and 19. Therefore, claims 13 and 19 are allowed."

Applicant appreciates the allowance of claims 13 and 19. Applicant respectfully submits that remaining claims are allowable in view of the amendments to the various claims as indicated with regard to the 35 U.S.C. §102(e) rejections.

Claim Rejections - 35 USC §102

Claims 1-12, 14-18, and 20-25 are rejected under 35 U.S.C. §102(e) as being anticipated by Dietz et al. (U.S. Patent No. 6,954,789, hereinafter "Dietz").

The purpose of the claimed invention is to speed up processing of Internet messages by concurrent operation of a FIFO buffer and an expression matching circuit.

Assuming *arguendo* that the FIFO buffer and expression matching circuit are the same as in the 35 USC §102 reference Dietz (USPN 6,954,789), Dietz has the expression matching circuit first and the FIFO buffer second for sequential operation. This may be seen in Dietz

FIGs. 3 and 11 where the parser 301 feeds the analyzer 303. The Dietz expression matching circuit is in the parser 301 and the UFKB (buffer) is in the analyzer 303.

Applicant's claim has the FIFO and the pattern matching of messages performed concurrently. Although it is believed to be apparent that the same message is being processed concurrently to speed up operation, the Applicant is amending the claims to clarify that the FIFO buffer and the pattern matching circuit are concurrently processing one message.

Independent claims 1, 7-8, 14, 20, and 25 have been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitation that there is an incoming message that is processed in the expression matching circuit concurrent with the processing in the FIFO:

> "a First-In-First-Out (FIFO) buffer adapted to receive the incoming message and to assemble the incoming message from a serial to a parallel form; and
> the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming message from a serial to a parallel form, recognize a Hypertext Transfer Protocol (HTTP) message header embedded in the incoming message, parse the recognized HTTP message header into a parsed HTTP message header, and provide the parsed HTTP message header to the server."

The support for the amendments is in Specification page 7, line 30, through page 8, line 7:

> "The present invention allows regular-expression pattern matching to be performed concurrently with the serial-to-parallel message-component assembly, such that message protocol header analysis can be done while incoming data is being clocked into the FIFO buffer 104. In this way, the message protocol header analysis incurs no extra time delay, and a compact representation of the extracted message protocol header information is ready for transfer to the web server 26 at the same time as the ordinary, assembled parts of the message. This technique may be referred to as "latency hiding"; i.e., overlapping some parts of a series of information processing steps in order to reduce the sequence's overall delay. The latency hiding technique has often been applied to the internal design of CPUs, but it is believed that it has not been previously applied to the present problem in the way described herein."

Dependent claims 2-4, 6, 9-12, and 15-17 have been amended to have proper antecedent bases in the independent claims from which they depend.

No new matter is being added.

It is respectfully submitted that the now amended independent claims 1, 7, 8, 14, 20, and 25, and the dependent claims depending therefrom, are not anticipated by Dietz under 35 USC §102(e).

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Claims 13 and 19 have been allowed. Allowance of claims 1-12, 14-18, and 20-25 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Registration No. 27,449

The Law Offices of Mikio Ishimaru
333 W. El Camino Real, Suite #330
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881
Date: December 4, 2006